TLV4110-EP, TLV4111-EP
TLV4112-EP, TLV4113-EP

SGLS314D–JUNE 2006–REVISED MAY 2008

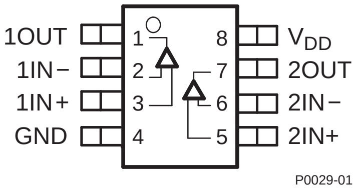
HIGH-OUTPUT-DRIVE OPERATIONAL AMPLIFIERS WITH SHUTDOWN

FEATURES

- **Controlled Baseline**
  - **One Assembly Site**
  - **One Test Site**
  - **One Fabrication Site**
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree** (1)
- **High Output Drive . . . >300 mA**
- **Rail-To-Rail Output**
- **Unity-Gain Bandwidth . . . 2.7 MHz**
- **Slew Rate . . . 1.5 V/µs**
- **Supply Current . . . 700 µA/Per Channel**
- **Supply Voltage Range . . . 2.5 V to 6 V**
- **Universal Op Amp EVM**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

TLV4112
D OR DGN PACKAGE
(TOP VIEW)



DESCRIPTION

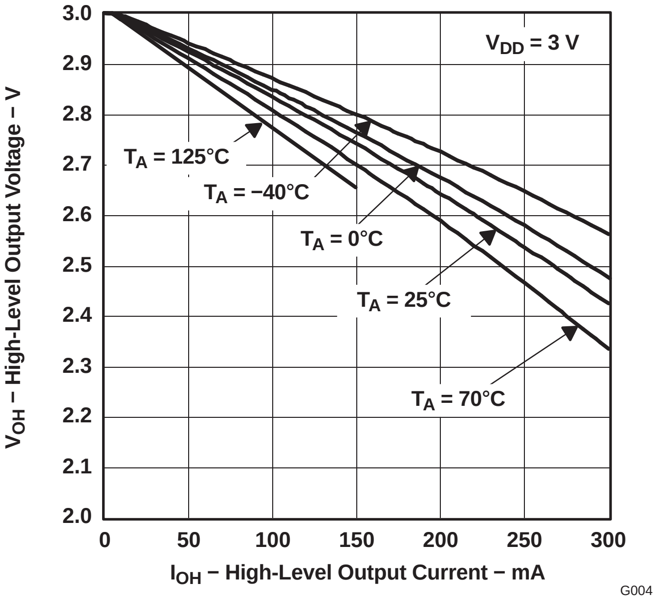
The TLV411x single-supply operational amplifiers provide output currents in excess of 300 mA at 5 V. This enables standard pin-out amplifiers to be used as high current buffers or in coil driver applications. The TLV4110 and TLV4113 come with a shutdown feature.

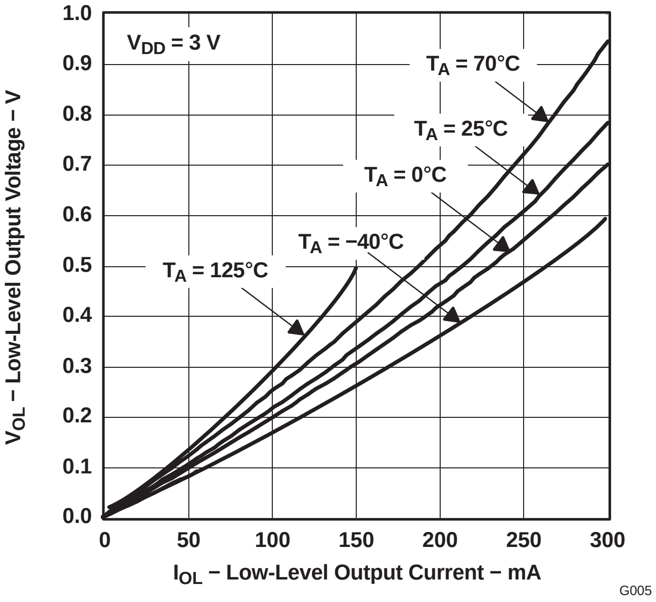
The TLV411x is available in the ultra-small MSOP PowerPAD™ package, which offers the exceptional thermal impedance required for amplifiers delivering high current levels.

All TLV411x devices are offered in SOIC (single and dual) and MSOP PowerPAD (dual).

FAMILY PACKAGE TABLE

DEVICE	NUMBER OF CHANNELS	PACKAGE TYPES		SHUTDOWN	UNIVERSAL EVM BOARD
		MSOP	SOIC		
TLV4110	1	8	8	Yes	See the EVM Selection Guide (SLOU060)
TLV4111	1	8	8	–	
TLV4112	2	8	8	–	
TLV4113	2	10	14	Yes	





TLV4110 AND TLV4111 AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		
	SMALL OUTLINE (D)(1) (2)	MSOP	
		SMALL OUTLINE (DGN)(1)	SYMBOL
–55°C to 125°C	TLV4110MDREP(3)	TLV4110MDGNREP(3)	BTB
	TLV4111MDREP(3)	TLV4111MDGNREP(3)	BTC

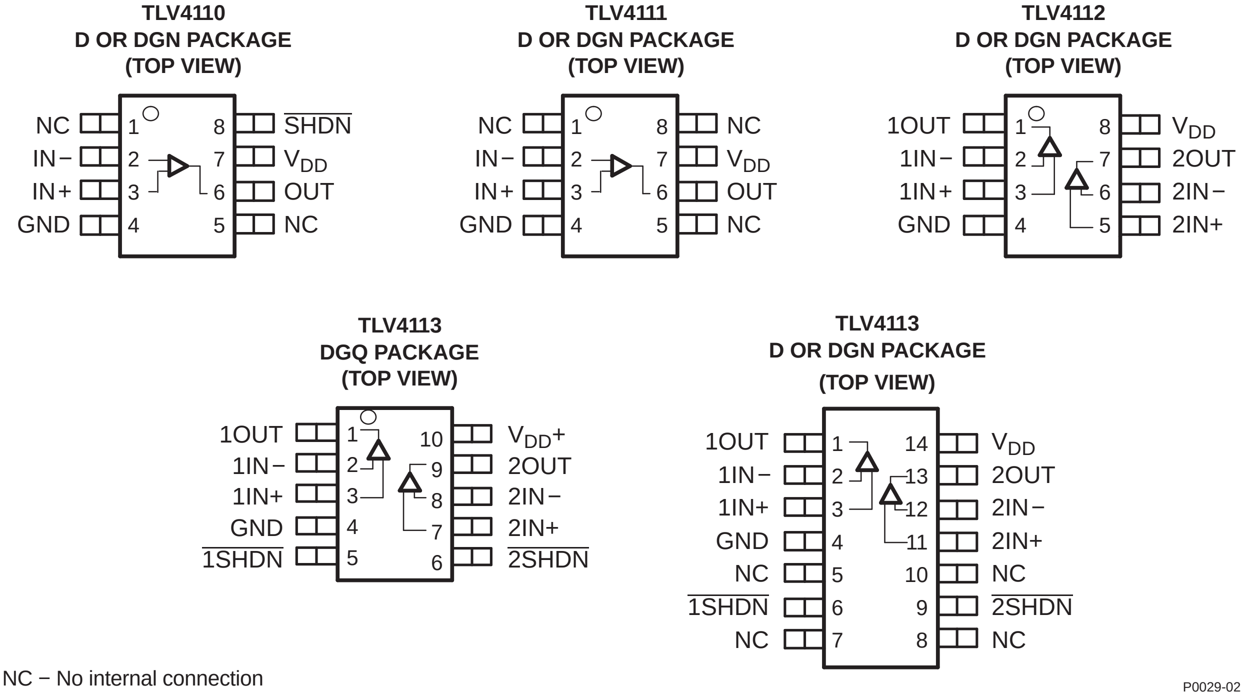
(1) The R designation indicates package is taped and reeled.
(2) In the SOIC package, the maximum RMS output power is thermally limited to 350 mW; 700 mW peaks can be driven, as long as the RMS value is less than 350 mW.
(3) Product preview.

TLV4112 AND TLV4113 AVAILABLE OPTIONS

T_A	PACKAGED DEVICES				
	SMALL OUTLINE (D) (1) (2)	MSOP			
		SMALL OUTLINE (DGN)(1)	SYMBOL	SMALL OUTLINE (DGQ)(1)	SYMBOL
–55°C to 125°C	TLV4112MDREP(3)	TLV4112MDGNREP(3)	BTD	–	–
	TLV4113MDREP(3)	–	–	TLV4113MDGQREP	BTE

(1) The R designation indicates package is taped and reeled.
(2) In the SOIC package, the maximum RMS output power is thermally limited to 350 mW; 700 mW peaks can be driven, as long as the RMS value is less than 350 mW.
(3) Product preview.

TLV411X PACKAGE PINOUTS



NC − No internal connection

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)[1]

V_{DD}	Supply voltage[2]		7 V
V_{ID}	Differential input voltage		$\pm V_{DD}$
V_I	Input voltage range		$\pm V_{DD}$
I_O	Output current[3]		800 mA
I_O	Continuous $\overline{\text{RMS}}$ output current (each output of amplifier)	$T_J \leq 105°C$	350 mA
		$T_J \leq 150°C$	110 mA
I_O	Peak output current (each output of amplifier	$T_J \leq 105°C$	500 mA
		$T_J \leq 150°C$	155 mA
	Continuous total power dissipation		See Dissipation Rating Table
T_A	Operating free-air temperature range		–55°C to 125°C
T_J	Maximum junction temperature		150°C
T_{stg}	Storage temperature range		–65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C

[1] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] All voltage values, except differential voltages, are with respect to GND.

[3] To prevent permanent damage, the die temperature must not exceed the maximum junction temperature.

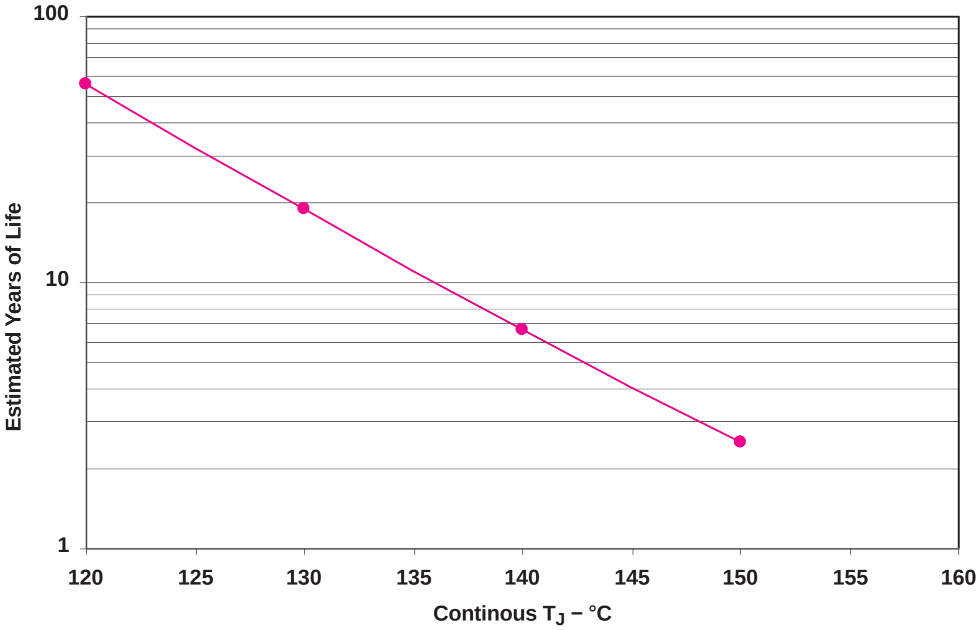


Figure 1. TLV4113MDGQ Wirebond Life

DISSIPATION RATING TABLE

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	$T_A \leq 25°C$ POWER RATING	$T_A = 25°C$ POWER RATING
D (8)	38.3	176	710 mW	142 mW
D (14)	26.9	122.3	1022 mW	204.4 mW
DGN (8)(1)	4.7	52.7	2.37 W	474.4 mW
DGQ (10)(1)	4.7	52.3	2.39 W	478 mW

(1) See the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout, based on information in the section entitled *Texas Instruments Recommended Board for PowerPAD*, on page 33 of SLMA002.

RECOMMENDED OPERATING CONDITIONS

				MIN	MAX	UNIT
V_{DD}	Supply voltage			2.5	6	V
V_{ICR}	Common-mode input voltage range			0	V_{DD} – 1.5	V
T_A	Operating free-air temperature			–55	125	°C
	Shutdown turnon/off voltage level[1]	V(on)	V_{DD} = 3 V	2.1		V
			V_{DD} = 5 V	3.8		
		V(off)	V_{DD} = 3 V		0.9	V
			V_{DD} = 5 V		1.65	

(1) Relative to GND

ELECTRICAL CHARACTERISTICS

at recommended operating conditions, V_{DD} = 3 V and 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A[1]	MIN	TYP	MAX	UNIT
DC PERFORMANCE								
V_{IO}	Input offset voltage	$V_{IC} = V_{DD}/2$, $V_O = V_{DD}/2$, R_L = 100 Ω, R_S = 50 Ω		25°C		175	3500	µV
				Full range			4000	
αVIO	Offset voltage drift			25°C		3		µV/°C
CMRR	Common-mode rejection ratio	V_{DD} = 3 V, R_S = 50 Ω, V_{IC} = 0 to 2 V		25°C		63		dB
		V_{DD} = 5 V, R_S = 50 Ω, V_{IC} = 0 to 4 V		25°C		68		
A_{VD}	Large-signal differential voltage amplification	V_{DD} = 3 V	R_L = 100 Ω	25°C	78	84		dB
				Full range	67			
			R_L = 10 kΩ	25°C	85	100		
				Full range	75			
		V_{DD} = 5 V	R_L = 100 Ω	25°C	88	94		
				Full range	75			
			R_L = 10 kΩ	25°C	90	110		
				Full range	85			
INPUT CHARACTERISTICS								
I_{IO}	Input offset current			25°C		0.3	25	pA
				Full range			1000	
I_{IB}	Input bias current			25°C		0.3	50	pA
				Full range			2000	
ri(d)	Differential input resistance			25°C		1000		GΩ
CIC	Common-mode input capacitance	f = 100 Hz		25°C		5		pF

(1) Full range is –55°C to 125°C.

ELECTRICAL CHARACTERISTICS (continued)

at specified free-air temperature, V_{DD} = 3 V and 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	MIN	TYP	MAX	UNIT
OUTPUT CHARACTERISTICS								
V_{OH}	High-level output voltage	V_{DD} = 3 V, $V_{IC} = V_{DD}/2$	I_{OH} = –10 mA	25°C	2.7	2.97		V
				Full range	2.6			
			I_{OH} = –100 mA	25°C	2.6	2.73		
				Full range	2.5			
		V_{DD} = 5 V, $V_{IC} = V_{DD}/2$	I_{OH} = –10 mA	25°C	4.7	4.96		V
				Full range	4.6			
			I_{OH} = –100 mA	25°C	4.6	4.76		
				Full range	4.5			
V_{OL}	Low-level output voltage	V_{DD} = 3 V and 5 V, $V_{IC} = V_{DD}/2$	I_{OL} = 10 mA	25°C		0.03	0.1	V
				Full range			0.2	
			I_{OL} = 100 mA	25°C		0.33	0.4	
				Full range			0.55	
I_O	Output current	Measured at 0.5 V from rail	V_{DD} = 3 V	25°C		±220		mA
			V_{DD} = 5 V			±320		
I_{OS}	Short-circuit output current	Sourcing		25°C		800		mA
		Sinking				800		
POWER SUPPLY								
I_{DD}	Supply current (per channel)	$V_O = V_{DD}/2$		25°C		700	1000	µA
				Full range			1500	
PSRR	Power supply rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	V_{DD} = 2.7 to 3.3 V, No load $V_{IC} = V_{DD}/2$ V		25°C	69	82		dB
				Full range	65			
		V_{DD} = 4.5 to 5.5 V, No load $V_{IC} = V_{DD}/2$ V		25°C	69	79		dB
				Full range	65			

(1) Full range is –55°C to 125°C.

ELECTRICAL CHARACTERISTICS (continued)

at specified free-air temperature, V_{DD} = 3 V and 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A[1]	MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE								
GBWP	Gain bandwidth product	R_L = 100 Ω, C_L = 10 pF		25°C		2.7		MHz
SR	Slew rate at unity gain	$V_{o(pp)}$ = 2.5 V, R_L = 100 Ω, C_L = 10 pF	V_{DD} = 3 V	25°C	0.8	1.57		V/µs
				Full range	0.4			
			V_{DD} = 5 V	25°C	1	1.57		
				Full range	0.5			
ϕM	Phase margin	R_L = 100 Ω, C_L = 10 pF		25°C		66		
	Gain margin	R_L = 100 Ω, C_L = 10 pF		25°C		16		dB
t_s	Settling time	$V(STEP)_{pp}$ = 1 V, A_V = –1, C_L = 10 pF, R_L = 100 Ω	0.1%	25°C		0.7		µs
			0.01%			1.3		
NOISE/DISTORTION PERFORMANCE								
THD+N	Total harmonic distortion, plus noise	$V_{O(pp)}$ = V_{DD}/2 V, R_L = 100 Ω, f = 100 Hz	A_V = 1	25°C		0.025		
			A_V = 10			0.035		
			A_V = 100			0.15		
V_n	Equivalent input noise voltage	f = 100 Hz		25°C		55		nV/√Hz
		f = 10 Hz				10		
I_n	Equivalent input noise current	f = 1 Hz		25°C		0.31		fA/√Hz
SHUTDOWN CHARACTERISTICS								
$I_{DD(SHDN)}$	Supply current in shutdown mode (per channel) (TLV4110, TLV4113)	$\overline{SHDN}$ = 0 V		25°C		3.4	10	µA
				Full range			15	
$t_{(ON)}$	Amplifier turnon time[2]	R_L = 100 Ω		25°C		1		µs
$t_{(Off)}$	Amplifier turnoff time[2]					3.3		

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(1) Full range is –55°C to 125°C.

(2) Disable time and enable time are defined as the interval between application of the logic signal to $\overline{SHDN}$ and the point at which the supply current has reached half its final value.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	vs Common-mode input voltage	2, 3
CMRR	Common-mode rejection ratio	vs Frequency	4
V_{OH}	High-level output voltage	vs High-level output current	5, 7
V_{OL}	Low-level output voltage	vs Low-level output current	6, 8
Z_o	Output impedance	vs Frequency	9
I_{DD}	Supply current	vs Supply voltage	10
k_{SVR}	Power supply voltage rejection ratio	vs Frequency	11
A_{VD}	Differential voltage amplification and phase	vs Frequency	12
	Gain-bandwidth product	vs Supply voltage	13
SR	Slew rate	vs Supply voltage	14
		vs Temperature	15
	Total harmonic distortion+noise	vs Frequency	16
V_n	Equivalent input voltage noise	vs Frequency	17
	Phase margin	vs Capacitive load	18
	Voltage-follower signal pulse response		19, 20
	Inverting large-signal pulse response		21
	Small-signal inverting pulse response		22
	Crosstalk	vs Frequency	23
	Shutdown forward and reverse isolation		24
	Shutdown supply current	vs Free-air temperature	25
	Shutdown supply current/output voltage		26

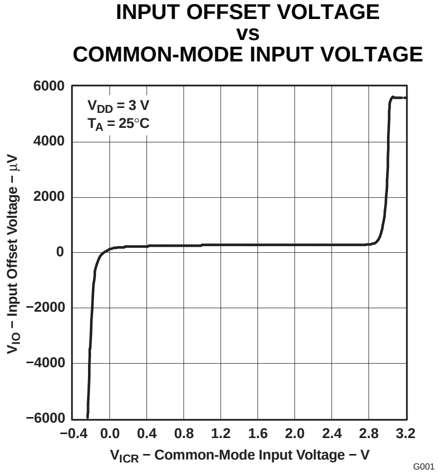

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

Figure 2.

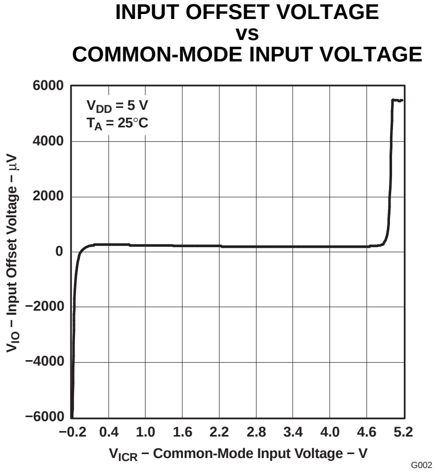

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

Figure 3.

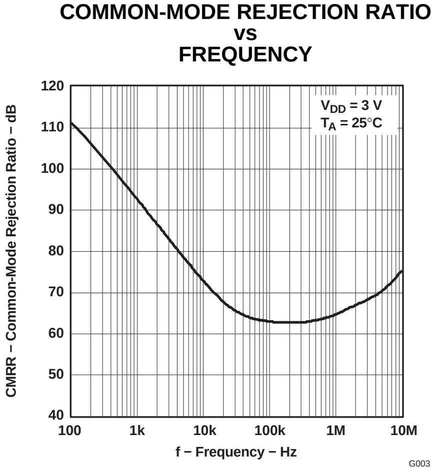

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

Figure 4.

**HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT**

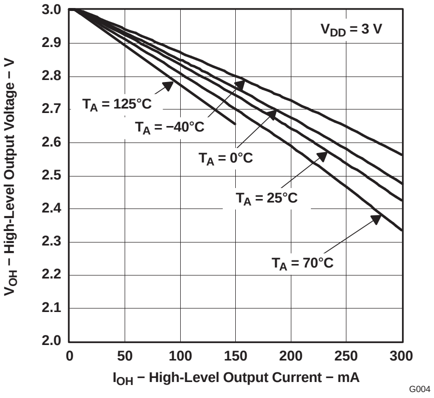


Figure 5.

**LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT**

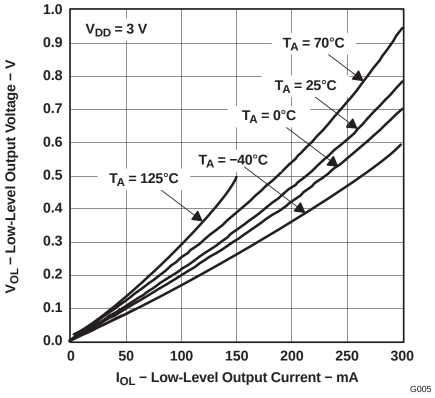


Figure 6.

**HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT**

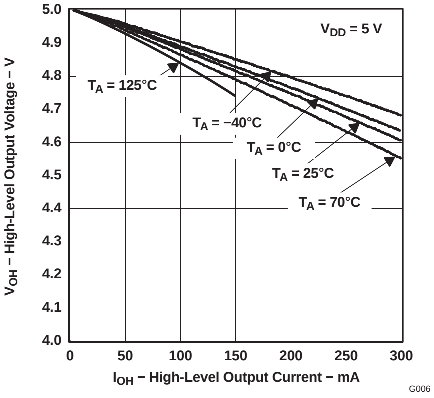


Figure 7.

**LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT**

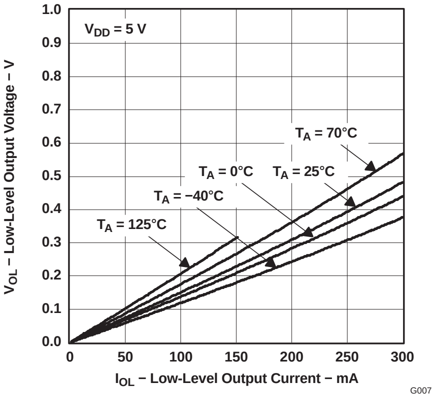


Figure 8.

**OUTPUT IMPEDANCE
vs
FREQUENCY**

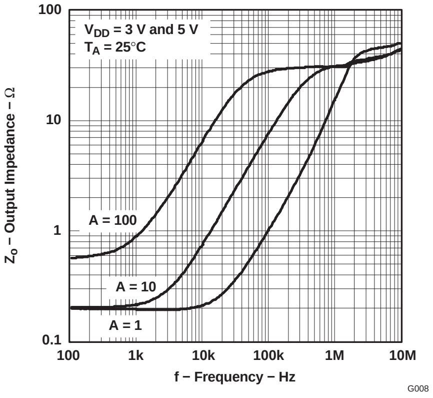


Figure 9.

**SUPPLY CURRENT
vs
SUPPLY VOLTAGE**

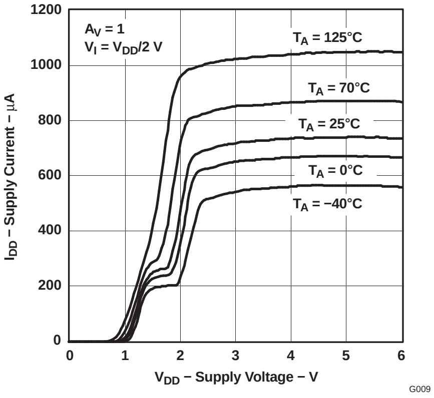


Figure 10.

**POWER-SUPPLY REJECTION
RATIO
vs
FREQUENCY**

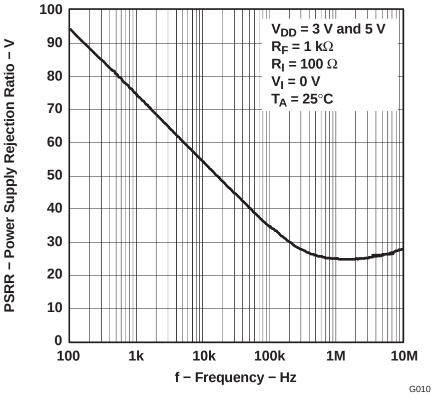


Figure 11.

**DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE
vs
FREQUENCY**

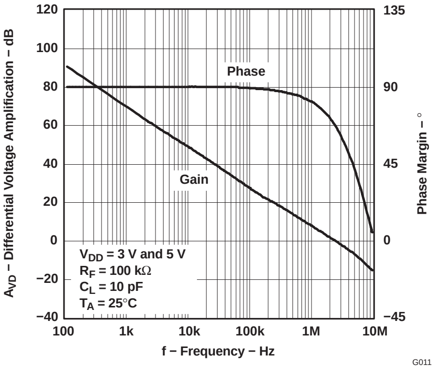


Figure 12.

**GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE**

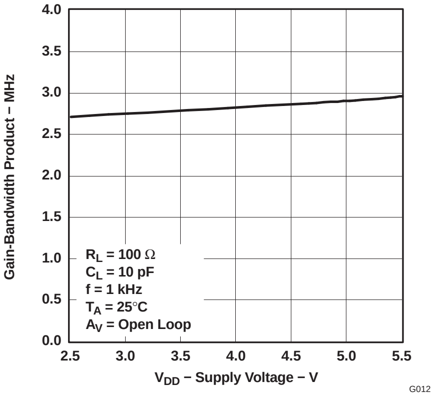


Figure 13.

SLEW RATE vs SUPPLY VOLTAGE

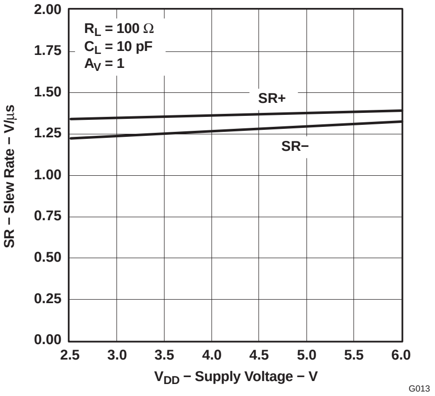


Figure 14.

SLEW RATE vs TEMPERATURE

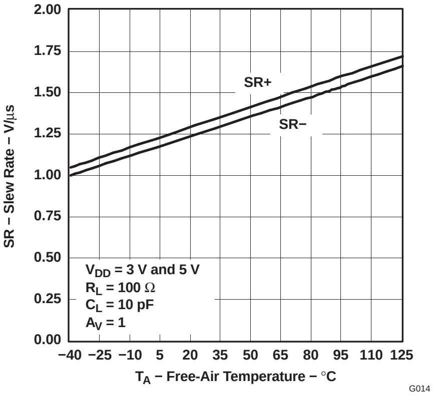


Figure 15.

TOTAL HARMONIC DISTORTION+NOISE vs FREQUENCY

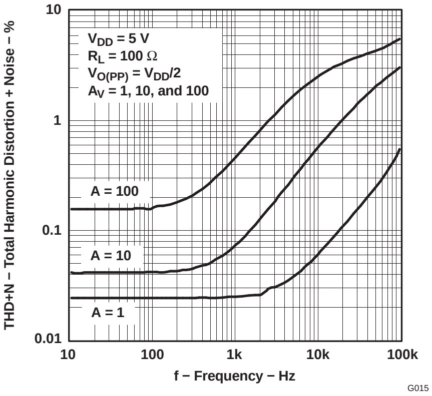


Figure 16.

EQUIVALENT INPUT VOLTAGE NOISE vs FREQUENCY

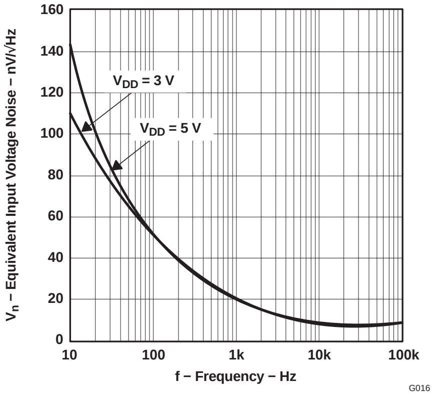


Figure 17.

PHASE MARGIN vs CAPACITIVE LOAD

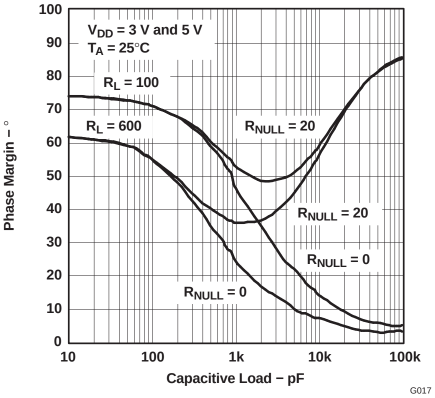


Figure 18.

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

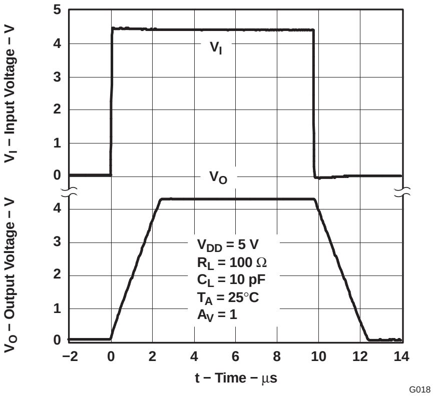


Figure 19.

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

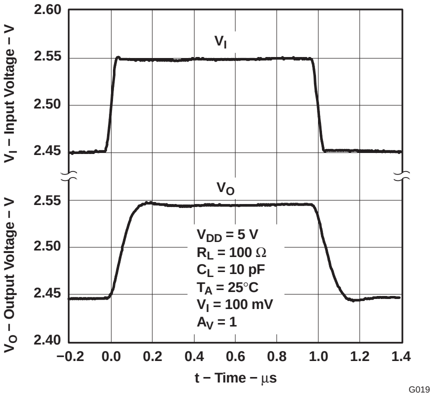


Figure 20.

INVERTING LARGE-SIGNAL PULSE RESPONSE

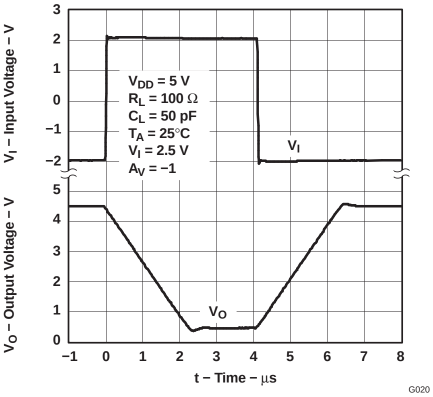


Figure 21.

SMALL-SIGNAL INVERTING PULSE RESPONSE

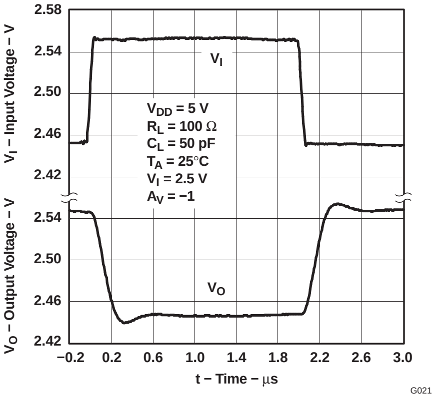


Figure 22.

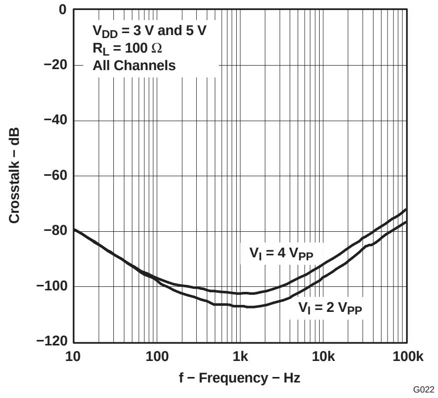

CROSSTALK
vs
FREQUENCY

Figure 23.

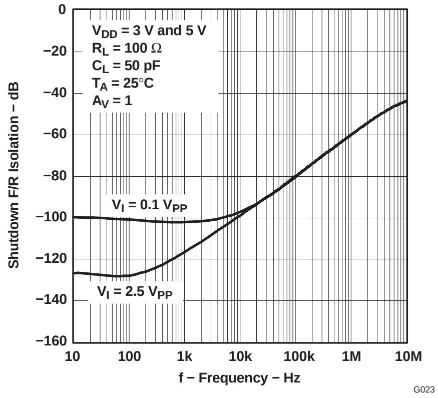

SHUTDOWN FORWARD AND
REVERSE ISOLATION

Figure 24.

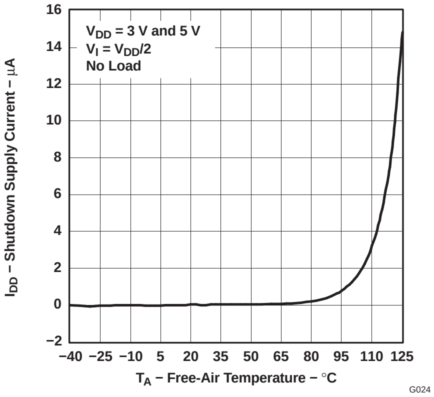

SHUTDOWN SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

Figure 25.

SHUTDOWN SUPPLY CURRENT / OUTPUT VOLTAGE

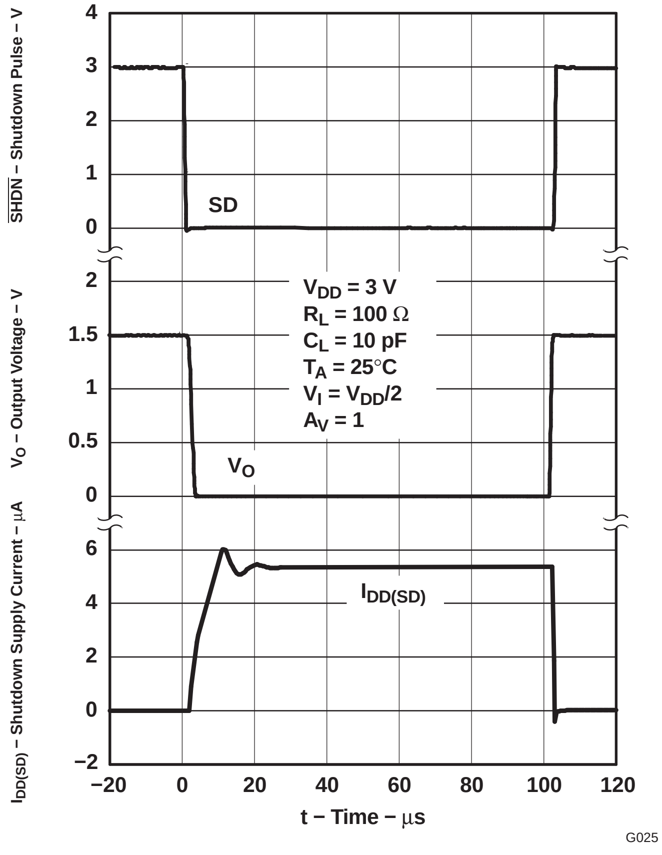


Figure 26.

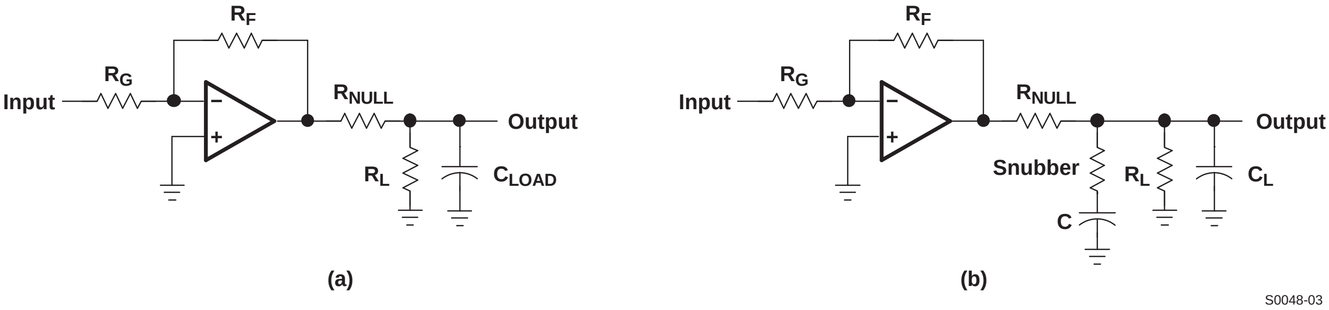
APPLICATION INFORMATION

SHUTDOWN FUNCTION

Two members of the TLV411x family (TLV4110/3) have a shutdown terminal for conserving battery life in portable applications. When the shutdown terminal is tied low, the supply current is reduced to just nano amps per channel, the amplifier is disabled, and the outputs are placed in a high-impedance mode. In order to save power in shutdown mode, an external pullup resistor is required; therefore, to enable the amplifier, the shutdown terminal must be pulled high. When the shutdown terminal is left floating, care should be taken to ensure that parasitic leakage current at the shutdown terminal does not inadvertently place the operational amplifier into shutdown.

DRIVING A CAPACITIVE LOAD

When the amplifier is configured in this manner, capacitive loading directly on the output decreases the device's phase margin, leading to high-frequency ringing or oscillations. Therefore, for capacitive loads of greater than 1 nF, it is recommended that a resistor be placed in series ®$_{NULL}$) with the output of the amplifier, as shown in Figure 27. A maximum value of 20 Ω is recommended for most applications.

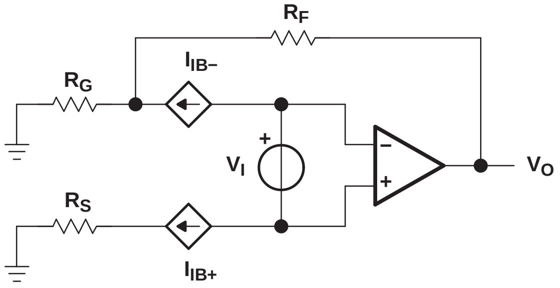


(a) (b)

Figure 27. Driving a Capacitive Load

OFFSET VOLTAGE

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage.



$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+}\, R_S\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-}\, R_F$$

S0094-01

Figure 28. Output Offset Voltage Model

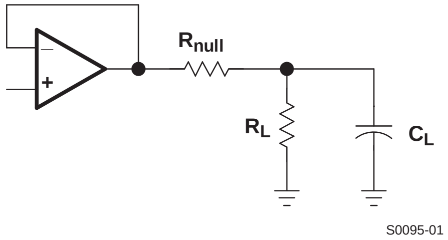


Figure 29.

GENERAL POWER DESIGN CONSIDERATIONS

When driving heavy loads at high junction temperatures there is an increased probability of electromigration affecting the long-term reliability of ICs. Therefore, to avoid this issue:

- The output current must be limited (at these high-junction temperatures).

OR

- The junction temperature must be limited.

The maximum continuous output current at a die temperature 150°C will be 1/3 of the current at 105°C.

The junction temperature will be dependent on the ambient temperature around the IC, thermal impedance from the die to the ambient and power dissipated within the IC.

$T_J = T_A + \theta_{JA} \times P_{DIS}$

Where:

P_{DIS} is the IC power dissipation and is equal to the output current multiplied by the voltage dropped across the output of the IC.

θ_{JA} is the thermal impedance between the junction and the ambient temperature of the IC.

T_J is the junction temperature.

T_A is the ambient temperature.

Reducing one or more of these factors results in a reduced die temperature. The 8-pin SOIC (small outline integrated circuit) has a thermal impedance from junction to ambient of 176°C/W. For this reason it is recommended that the maximum power dissipation of the 8-pin SOIC package be limited to 350 mW, with peak dissipation of 700 mW as long as the RMS value is less than 350 mW.

The use of the MSOP PowerPAD™ dramatically reduces the thermal impedance from junction to case. And, with correct mounting, the reduced thermal impedance greatly increases the IC's permissible power dissipation and output current handling capability. For example, the power dissipation of the PowerPAD™ is increased to above 1 W. Sinusoidal and pulse-width modulated output signals also increase the output current capability. The equivalent dc current is proportional to the square-root of the duty cycle:

$$I_{DC(EQ)} = I_{Cont} \times \sqrt{(\text{duty cycle})} \tag{1}$$

CURRENT DUTY CYCLE AT PEAK RATED CURRENT	EQUIVALENT DC CURRENT AS A PERCENTAGE OF PEAK
100	100
70	84
50	71

Note that, with an operational amplifier, a duty cycle of 70% often results in the op-amp sourcing current 70% of the time and sinking current 30%; therefore, the equivalent dc current is still 0.84 times the continuous current rating at a particular junction temperature.

GENERAL PowerPAD DESIGN CONSIDERATIONS

The TLV411x is available in a thermally-enhanced PowerPAD family of packages. These packages are constructed using a downset lead frame upon which the die is mounted [see Figure 30(a) and Figure 30(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 30(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the previously awkward mechanical methods of heat sinking.

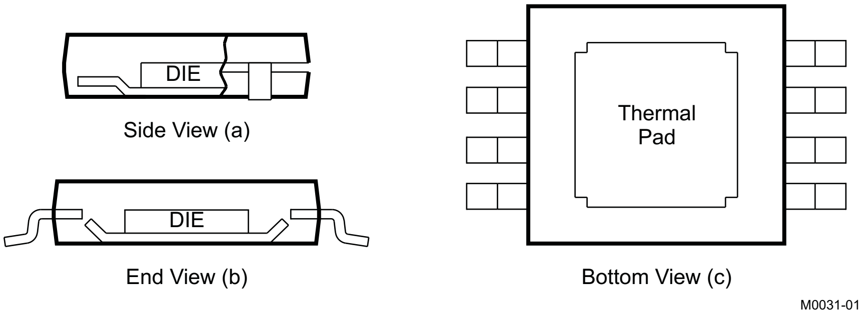


Figure 30. Views of Thermally Enhanced DGN Package

Although there are many ways to properly heatsink the PowerPAD package, the following steps illustrate the recommended approach.

1. Prepare the PCB with a top-side etch pattern, as shown in Figure 31. There should be etch for the leads as well as etch for the thermal pad.
2. Place five holes (dual) or nine holes (quad) in the area of the thermal pad. These holes should be 13 mils in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the TLV411x IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal-resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the TLV411x PowerPAD package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes (dual) or nine holes (quad) exposed. The bottom-side solder mask should cover the five or nine holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the TLV411x IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

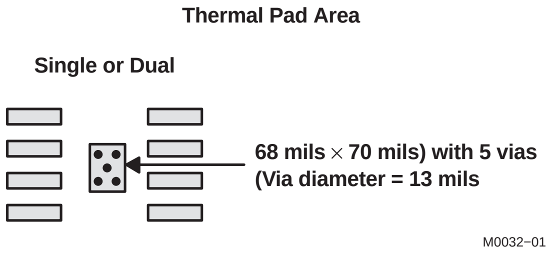


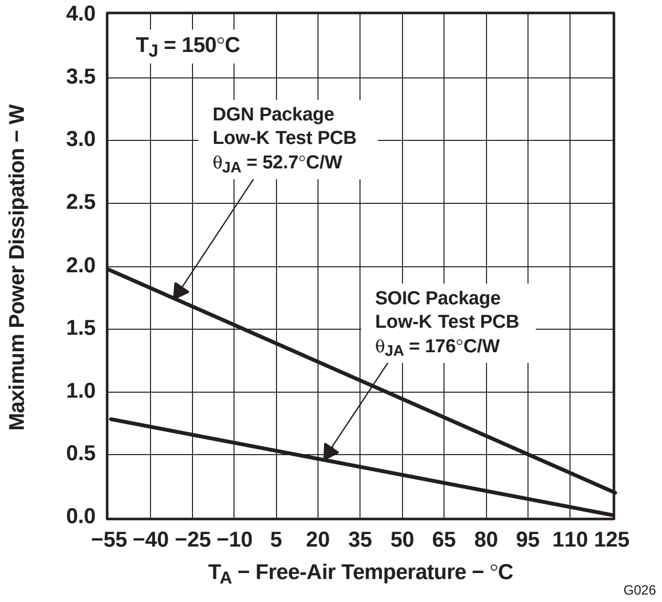
Figure 31. PowerPAD PCB Etch and Via Pattern

For a given θ_{JA}, the maximum power dissipation is shown in Figure 32 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}}\right)$$

Where:

P_D = Maximum power dissipation of TLV411x IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case
θ_{CA} = Thermal coefficient from case to ambient air (°C/W) (2)



NOTE: Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 32. Maximum Power Dissipation vs Free-Air Temperature

The next consideration is the package constraints. The two sources of heat within an amplifier are quiescent power and output power. The designer should never forget about the quiescent heat generated within the device, especially multi-amplifier devices. Because these devices have linear output stages (Class A-B), most of the heat dissipation is at low output voltages with high output currents.

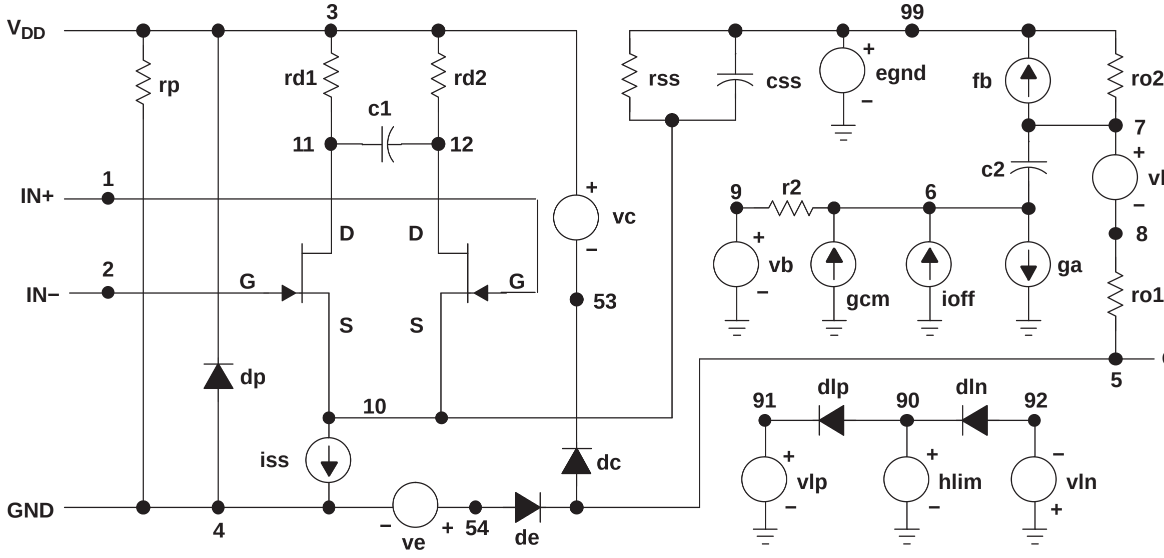
The other key factor when dealing with power dissipation is how the devices are mounted on the PCB. The PowerPAD devices are extremely useful for heat dissipation. But, the device should always be soldered to a copper plane to fully use the heat dissipation properties of the PowerPAD. The SOIC package, on the other hand, is highly dependent on how it is mounted on the PCB. As more trace and copper area is placed around the device, θ_{JA} decreases and the heat-dissipation capability increases. The currents and voltages shown in these graphs are for the total package. For the dual or quad amplifier packages, the sum of the RMS output currents and voltages should be used to choose the proper package.

MACROMODEL INFORMATION

Macromodel information provided was derived using Microsim Parts™, the model generation software used with Microsim PSpice™ The Boyle macromodel (see Note 3) and subcircuit in Figure 33 are generated using the TLV411x typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases).

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 3: G.R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers," IEEE Journal of Solid-State Circuits, SC-9, 353 (1974).



```
* TLV4112_5V operational amplifier ”macromodel” subcircuit
* updated using Model Editor release 9.1 on 01/18/00 at 15:50
Model Editor is an OrCAD product.
*
* connections:   non−inverting input
*                               | inverting input
*                               | |  positive power supply
*                        | | |  negative power supply
*                        | |  |  |  output
*                               | | |  | |
.subckt TLV4112_5V       1 2 3 4 5
*
             c1        11     12     2.2439E−12
             c2        6      7      10.000E−12
             css       10     99     454.55E−15
             dc        5      53     dy
             de        54     5      dy
             dlp       90     91     dx
             dln       92     90     dx
             dp        4      3      dx
             egnd      99     0      poly(2) (3,0) (4,0) 0 .5 .5
             fb        7      99     poly(5) vb vc ve vlp vln 0
             + 33.395E6 −1E3 1E3 33E6 −33E6
             ga        6      0      11     12   168.39E−6
             gcm       0      6      10     99   168.39E−12
```

```
iss          10     4      dc          13.800E−6
hlim         90     0      vlim 1K
ioff         0      6      dc          75E−9
j1           11     2      10 jx1
J2           12     1      10 jx2
r2           6      9      100.00E3
rd1          3      11     5.9386E3
rd2          3      12     5.9386E3
ro1          8      5      10
ro2          7      99     10
rp           3      4      3.3333E3
rss          10     99     14.493E6
vb           9      0      dc 0
vc           3      53     dc .86795
ve           54     4      dc .86795
vlim         7      8      dc 0
vlp          91     0      dc 300
vln          0      92     dc 300
.model       dx     D(Is=800.00E−18)
.model       dy     D(Is=800.00E−18 Rs=1m Cjo=10p)
.model       jx1    NJF(Is=150.00E−12 Beta=2.0547E−3 +Vto=−1)
.model       jx2    NJF(Is=150.00E−12 Beta=2.0547E−3 + Vto=−1)
.ends
*$
```

S0096-01

Figure 33. Boyle Macromodel and Subcircuit

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV4113MDGQREP	ACTIVE	HVSSOP	DGQ	10	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-1-260C-UNLIM	-55 to 125	BTE	Samples
V62/06646-04ZE	ACTIVE	HVSSOP	DGQ	10	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-1-260C-UNLIM	-55 to 125	BTE	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TLV4113-EP :

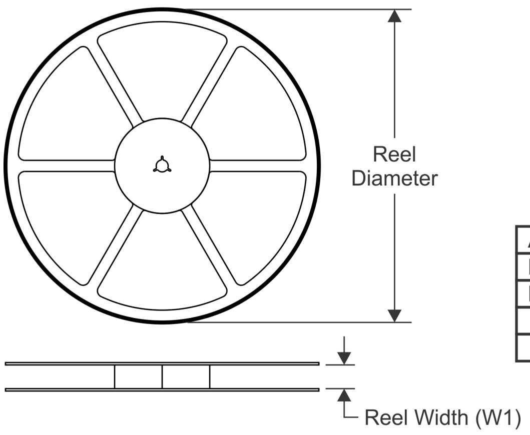
- Catalog: TLV4113

NOTE: Qualified Version Definitions:

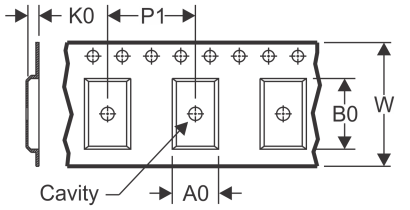
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

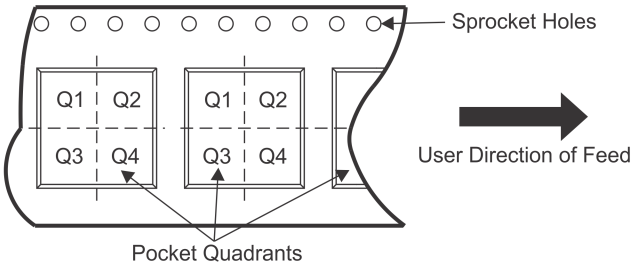


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

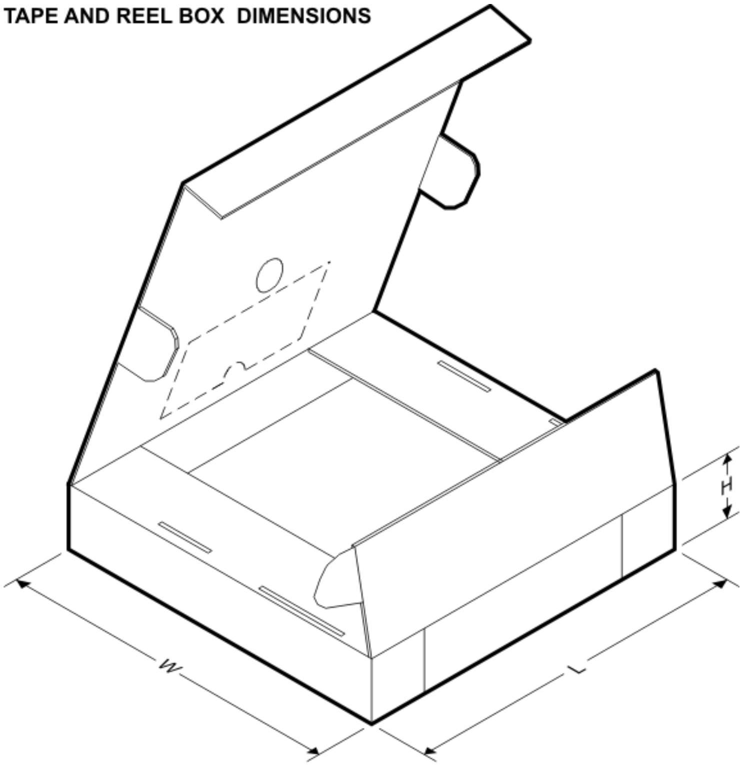
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV4113MDGQREP	HVSSOP	DGQ	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

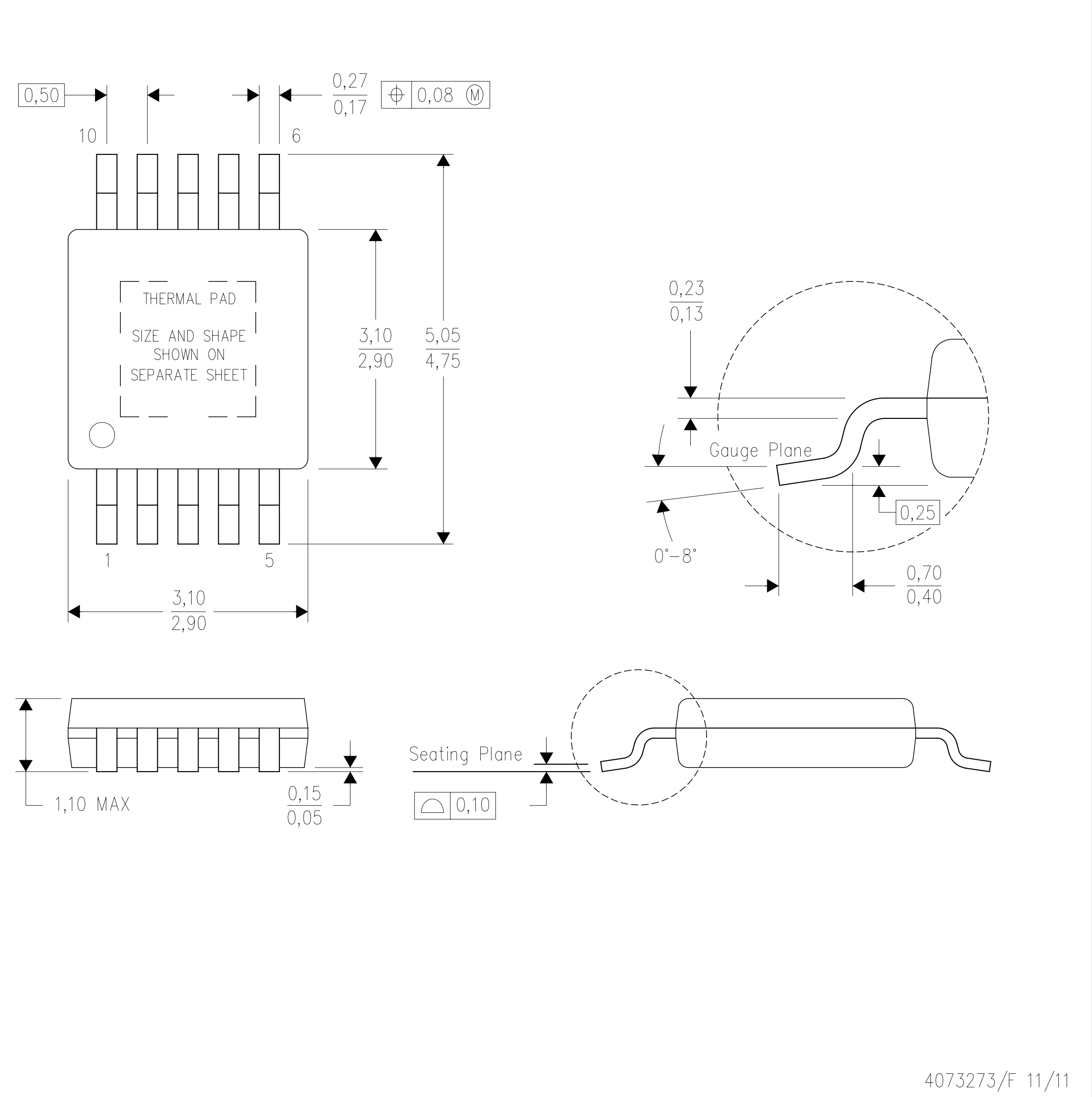
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV4113MDGQREP	HVSSOP	DGQ	10	2500	358.0	335.0	35.0

DGQ (S-PDSO-G10) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO-187 variation BA-T.

PowerPAD is a trademark of Texas Instruments.

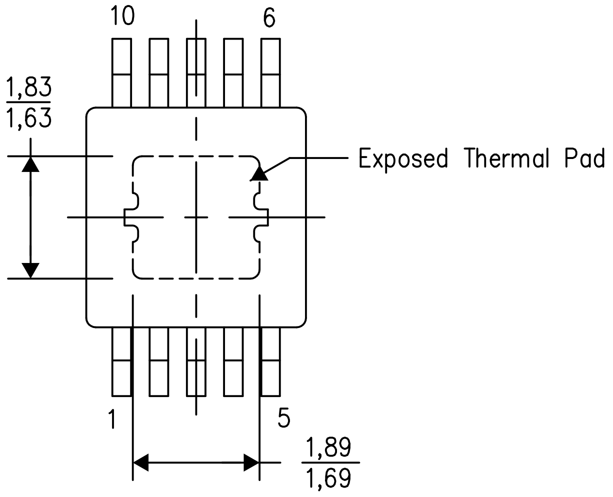
DGQ (S-PDSO-G10) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

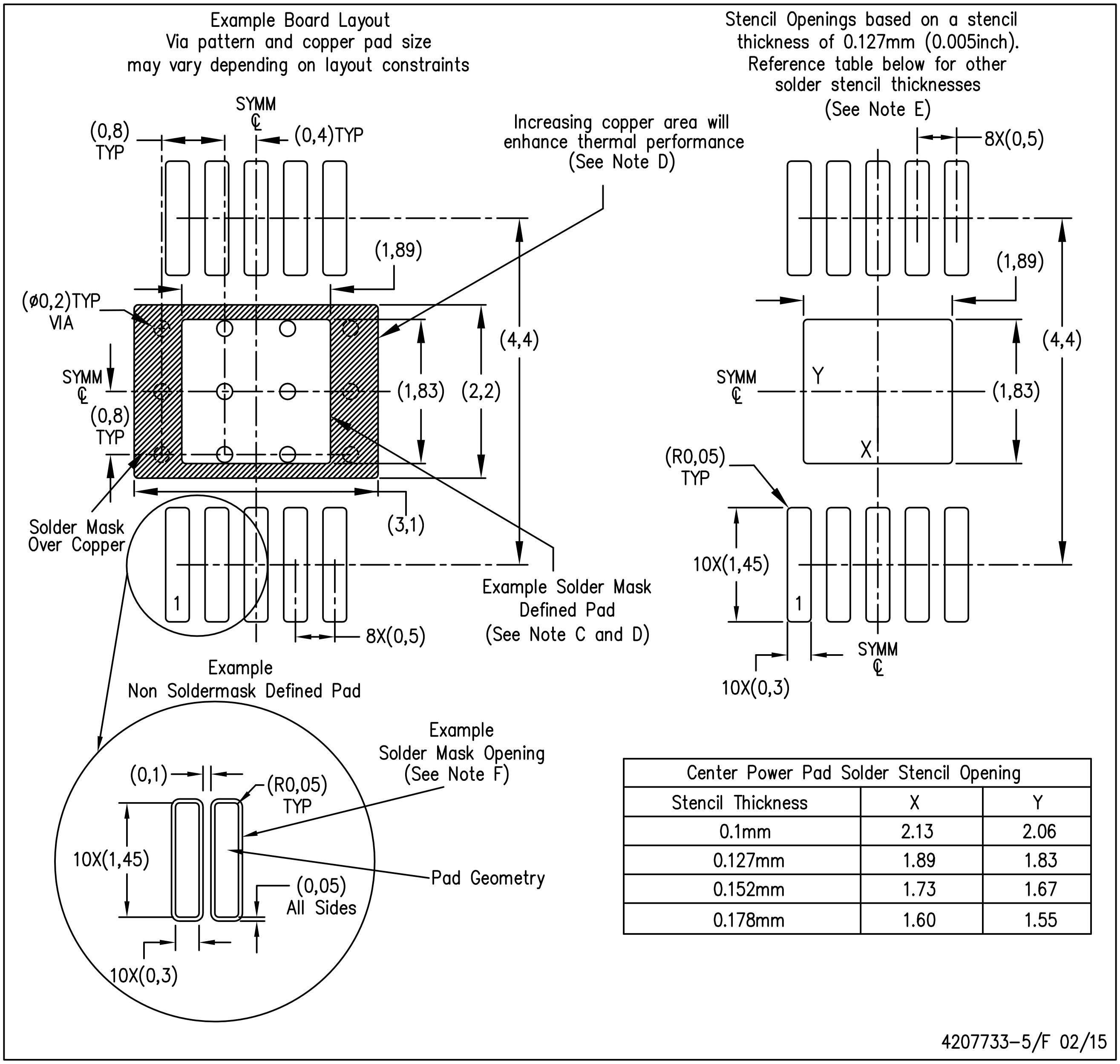
Exposed Thermal Pad Dimensions

4206324-7/H 12/14

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DGQ (S–PDSO–G10) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.13	2.06
0.127mm	1.89	1.83
0.152mm	1.73	1.67
0.178mm	1.60	1.55

4207733–5/F 02/15

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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